REMARKS

The application is believed to be in condition for allowance for the reasons set forth below.

Claims 1-22 are pending in the application.

Claims 1, 2, 6-8, 11-18, 20 and 21 were rejected under 35 USC §102(e) as being anticipated by KANEKAR et al. 6,751,191. That rejection is respectfully traversed.

Claims 1, 13-15 and 18 are the independent claims.

Each of the independent claims includes the features:

"wherein said configurable integrated circuit of said protecting pair unit of said data computing device is structured and arranged to perform the switch-over independently of a CPU, when the switch-over is needed".

The Office Action offers Figure 14 of KANEKAR as disclosing this feature.

However, neither this figure nor any other portion of KANEKAR discloses or suggests the recited structure and configuration.

To the contrary, KANEKAR discloses a central CPU based switch-over. Such a system is disclosed and disparaged on page 1, line 31 to page 2, line 14 of the present application and is the type of system the present claims define over.

Typically the need for the switch-over is communicated via micro-processors as is done is KANEKAR. When a working connection (W) becomes faulty, an interrupt request is given to a microprocessor (CPU). After receiving the interrupt request, the CPU on the working side unit signals the CPU on the protection side unit, which then switches the traffic of the connection to a protecting connection (P). The system of KANEKAR may have some configurable integrated circuit (IC) such as application-specific integrated circuit (ASIC) but not for the switch-over process, and the CPU's presence is crucial.

For example, column 17 of KANEKAR disclose the structure and configurations of the router used in KANEKAR. On column 17, line 14 onwards, a master central processing unit (CPU) based switch over structure and configuration is described. Furthermore, master microprocessor 1462 effectively performs these functions as stated on column 17, line 54. Also CPU is responsible for router task, i.e. the switch-over, etc. as in column 17, lines 17 - 18.

Further details as to how the recited invention differs over KANEKAR are set forth below that show that the Official Action has mischaracterized KANEKAR's invention.

As set forth above, KANEKAR is based on using CPU's to handle the protection switch-over. This is described in KANEKAR

as the typical way of handling the protection switch-over. However, KANEKAR does not recognize the disadvantage that this traditional switch-over based on CPU's communication is slow. Improving this switch-over time is just what the present invention is all about by handling the switch-over in HW (=IC, ASIC, FPGA).

The position set forth in the Official Action is that KANEKAR teaches in column 5, lines 49-60 that the switch-over of KANEKAR is less than 50 ms. Nowhere in these lines, indeed nowhere in the whole patent of KANEKAR, is there anything mentioned about switchover being done in less than 50 ms.

Additionally, the position set forth in the Official Action is that e.g. Fig 12A shows that when the master fails it would signal to slave as step 1202 without CPU. However, this does not occur. Rather, upon reading the whole text in KANEKAR related to Figure 12A, that is column 11, lines 55-67 and column 12, lines 1-22 it is apparent that the switch-over is commanded and controlled by a CPU.

Applicant's position that the switch-over in KANEKAR is commanded and controlled by a CPU is further evidenced by the following passages of KANEKAR.

First, KANEKAR defines in column 11, lines 55-58 what he means with hardware and software: " …a failure of the hardware (i.e. switching engine) or software (i.e. routing processor or switch processor) in a router is treated as failure of the entire router". As defined with this statement KANEKAR highlights that the routing processor and switch processor are SW i.e. CPUs.

Second, looking at Figure 5 of KANEKAR together with the text in column 7, lines 32-35, KANEKAR explains that the router includes both in the master device as well as in the slave device 2 CPUs, the routing processor 506 and 508 and the switching processor 510 and 512 as well as a forwarding engine 514 and 516. The forwarding engine is the HW (= IC, ASIC, FPGA) as described in column 7, lines 46-48 "The forwarding engines 514 and 516 may perform forwarding in hardware and therefore each functions as a switch."

Note that KANEKAR describes in column 7, lines 35-36 that processor controls the forwarding engine: "the routing processors 506 and 508 run the layer 3 protocols" and in column 7, lines 36-41: "In addition, since the device also functions as a bridge, the switch processors 510 and 512 are adapted for handling the layer 2 protocols (e.g. spanning tree protocol) and may therefore control the hardware by initializing the associated forwarding engines 514 and 516."

KANEKAR also explains in column 8, lines 1-3 that "In addition, each of the forwarding engines, 514 and 516 maintains its own tables, which will be described below with reference to FIGS. 13A through 13C."

Finally, in column 11, lines 55-67 and column 12, lines 1-22, KANEKAR explains how upon a failure the switch-over to slave is done. Reading this text and referring to the Figures, one can see that the switch-over is controlled with the processors.

For example, column 11, lines 61-63 "Upon failure of the master at 1200, a backplane signal is sent to the slave block 1202. The slave then starts the layer 2 spanning tree protocols at block 1204." and further at column 12, lines 11-15 "Thus, at block 1208, the routing processor of the slave sends a signal to the forwarding engine to replace the references to the MAC address and IP address of the master with the MAC address and IP address of the slave, where appropriate."

Throughout KANEKAR, it is clear, as outlined above, that the switch-over decision making is done in a processor, CPU, which commands the hardware, forwarding engine, to do the switch-over.

In view of the above, it is apparent that one having ordinary skill in the design engineering art reading KANEKAR, would not understand this reference to include a configurable integrated circuit of a protecting pair unit of a data computing device that is structured and arranged to perform a switch-over independently of a CPU, when the switch-over is needed.

Accordingly, it is apparent that KANEKAR does not disclose that which is recited and reconsideration and withdrawal of the rejection are respectfully requested.

Claims 3-5, 9, 10 and 22 were rejected under 35 USC 103(a) as being unpatentable over KANEKAR et al. in view of SHABTAY et al. 7,093,027. That rejection is respectfully traversed.

SHABTAY is only cited with respect to features of the dependent claims. SHABTAY does not overcome the shortcomings of KANEKAR set forth above with respect to claim 1. Since claims 3-5, 9, 10 and 22 depend from claim 1 and further define the invention, these claims are believed to be patentable at least for depending from an allowable independent claim.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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